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10/043,047	01/09/2002	Chang-Sik Yoo	SAM-0204	5014

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EXAMINER	
CHEN, TSE W	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,047	YOO ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-65* is/are pending in the application.

4a) Of the above claim(s) *16-21,25-53,58,59 and 62-64* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,22-24,54-57,60,61 and 65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *010902,111204*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of species of Group A, "memory system with claimed operations based on clock signals", in the reply filed on June 9, 2005 is acknowledged. However, Applicant's listing of claims readable on the elected species contains claims 16-21 and 62, drawn to another species of Group A, "memory system with claimed operations based on *flag* signals". Accordingly, Examiner will prosecute claims 1-15, 22-24, 54-57, 60-61, and 65, readable on the elected species of "memory system with claimed operations based on clock signals".

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on January 9, 2002 and November 12, 2004 were filed before the mailing date of the first Office Action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 54-56 and 65 are rejected under 35 U.S.C. 102(e) as being anticipated by Gillingham et al., US Patent 6510503, hereinafter Gillingham.

5. In re claim 54, Gillingham discloses a memory system [80] having a stub configuration [col.10, l.58 – col.11, l.8] comprising:

- A controller [82] for generating a first clock signal [86], a control signal [col/row], an address signal [col.3, ll.1-12] and data signals on a data bus, the data bus, first clock signal, control signal, and address signal being arranged in a stub configuration [col.10, l.10 – col.11, l.8; col.12, ll.1-12; fig.7].
- A second clock signal generator [107, 108] for generating a second clock signal [outclk, dclk] [col.10, 40-45; col.11, ll.23-49].
- A memory module [170] including memory devices [100, 174] coupled to the controller, the memory module receiving the first clock signal, the second clock signal and the control signal that includes a read or write command [col.2, ll.16-47; col.10, ll.10-23; col.11, ll.23-49; fig.13, 14].
- The first clock signal propagating from the controller to the memory module in a first direction of propagation, and the second clock signal propagating from the memory module to the controller in a second direction of propagation [col.10, ll.10-23, ll.49-53; col.11, ll.23-49; 86 propagates from controller to module and dclk propagates from module to controller in a read operation].
- The memory module, in response to the write command, initiating a write operation for writing the data signals from the data bus to the memory devices in synchronization with the first clock signal [col.10, ll.49-53; uses 86 to write data].
- The memory module, in response to the read command, initiating a read operation for reading data from the memory devices to the data bus in response to the second clock

signal, the controller receiving the data signals on the data bus in response to the second clock signal during the read operation [col.11, ll.23-49].

6. As to claim 55, Gillingham discloses, wherein the first clock signal comprises a write clock and wherein the second clock signal comprises a read clock [col.10, ll.49-53; col.11, ll.23-49].

7. As to claim 56, Gillingham discloses, wherein the memory controller further compensates for phase difference between the received second clock signal and the data signals on the data bus [col.13, ll.20-37].

8. In re claim 65, Gillingham discloses each and every limitation as discussed above in reference to claim 54. Gillingham discloses the memory system; therefore, Gillingham discloses the method of operating the memory system.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-4, 6-9, 11 and 60-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, in view of Keeth, US Patent 6029250.

11. Gillingham discloses a memory system [80] having a stub configuration [col.10, l.58 – col.11, l.8] comprising:

- A controller [82] for generating a first clock signal [86], a control signal [col/row], an address signal [col.3, ll.1-12] and data signals on a data bus, the data bus, first clock

signal, control signal, and address signal being arranged in a stub configuration [col.10, l.10 – col.11, l.8; col.12, ll.1-12; fig.7].

- A memory module [170] including memory devices [100, 174] coupled to the controller, the memory module receiving the first clock signal and the control signal that includes a read or write command [col.2, ll.16-47; fig.13, 14].
- The memory module, in response to the write command, initiating a write operation for writing the data signals from the data bus to the memory devices in synchronization with the first clock signal [col.10, ll.49-53; uses 86 to write data].
- The memory module, in response to the read command, initiating a read operation for reading data from the memory devices to the data bus [col.11, ll.23-49].
- The controller receiving the data signals on the data bus during the read operation [col.10, ll.40-57].

12. Gillingham did not discuss the details of clock generations in the memory module.

13. Keeth discloses a memory system [fig.4] comprising a memory module [404], in response to a read command, initiating a read operation for reading data from memory devices [80a-h] to a data bus [dq] in synchronization with a first clock signal [rclk] and generating a second clock signal [dclk0/1] in response to the first clock signal, the second clock signal being provided to a controller [402], the controller receiving the data signals on the data bus in response to the second clock signal during the read operation [col.10, ll.26-39; col.13, ll.8-23; col.14, ll.41-60].

14. It would have been obvious to one of ordinary skill in the art, having the teachings of Gillingham and Keeth before him at the time the invention was made, to modify the memory

module taught by Gillingham to include the teachings of Keeth, in order to obtain the memory system comprising the memory module that, in response to the read command, initiating a read operation for reading data from the memory devices to the data bus in synchronization with the first clock signal and generating a second clock signal in response to the first clock signal, the second clock signal being provided to the controller, the controller receiving the data signals on the data bus in response to the second clock signal during the read operation.. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to better synchronize memory access of increasing number of memory modules [Keeth: col.1, l.17 – col.2, l.14; col.7, ll.28-52].

15. As to claim 2, Gillingham discloses, wherein the first clock signal [86] comprises a write clock [col.10, ll.49-53] and Keeth discloses, wherein the second clock signal comprises a read clock [rclk].

16. As to claim 3, Keeth discloses, wherein the system comprises multiple memory modules and wherein the multiple memory modules each generate independent second clock signals, the second clock signals each being different in phase [col.7, ll.6-52].

17. As to claim 4, Keeth discloses, wherein the phases of the multiple second clock signals are different in phase due to the difference in propagation delay between each of the memory modules and the controller [col.5, l.34 – col.6, l.23].

18. As to claim 6, Keeth discloses, wherein the memory module further includes a control/address buffer [46, 420 and associated units constitute the buffer] that receives the first clock signal and the control signal and generates the second clock signal in response to the first clock signal [col.14, ll.41-60].

19. As to claim 7, Gillingham discloses, wherein the memory module further includes a phase locked loop that receives the first clock signal and generates the second clock signal in response to the first clock signal [col.2, ll.10-13].

20. As to claim 8, Gillingham discloses, wherein the memory module further includes a delay locked loop that receives the first clock signal and generates the second clock signal in response to the first clock signal [col.2, ll.10-13].

21. As to claim 9, Gillingham discloses, wherein the memory module includes a return path that is coupled to a first clock signal line that receives the first clock signal for generating the second clock signal in response to the first clock signal [fig.6a; cfc loops to ctc].

22. As to claim 11, Keeth discloses, wherein the memory system includes first and second memory modules, the memory module generating respective first and second independent return clock signals as the second clock signal [col.7, ll.6-52]; and Gillingham discloses, further comprising a motherboard [180] coupling the first and second memory modules and the controller, the motherboard including the data bus, a control bus for transfer of the control signal; an address bus for transfer of the address signal; a first clock signal line for transfer of the first clock signal and first and second independent return clock signal lines for transfer of the first and second return clock signals [fig.7, 13a; col.15, l.65 – col.16, l.11; main bus comprising of lines necessary to transfer control/address/data/clock signals].

23. In re claim 60, Gillingham and Keeth disclose each and every limitation as discussed above in reference to claim 1. Gillingham and Keeth discloses the memory system; therefore, Gillingham and Keeth discloses the method of operating the memory system.

24. In re claim 61, Gillingham and Keeth disclose each and every limitation as discussed above in reference to claims 3 and 60.

25. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham and Keeth as applied to claim 1 above, and further in view of Gasbarro et al., US Patent 5432823, hereinafter Gasbarro.

26. Gillingham and Keeth taught each and every limitation as discussed above in reference to claim 1. Gillingham and Keeth did not disclose explicitly that the propagation delay of the second clock signal from the memory module to the controller is substantially equal to that of the data bus.

27. Gasbarro discloses a system wherein the propagation delay of a clock signal from a module [device] to a controller [master] is substantially equal to that of a data bus [120] [col.5, ll.18-20].

28. It would have been obvious to one of ordinary skill in the art, having the teachings of Gillingham, Keeth and Gasbarro before him at the time the invention was made, to modify the memory system taught by Gillingham and Keeth to include the teachings of Gasbarro, in order to obtain the memory system wherein the propagation delay of the second clock signal from the memory module to the controller is substantially equal to that of the data bus. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to alleviate problems with clock data-skew [Gasbarro: col.2, l.9 – col.3, l.5].

29. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham and Keeth as applied to claim 9 above, and further in view of Moyal et al., US Patent 6326853, hereinafter Moyal.

30. Gillingham and Keeth taught each and every limitation as discussed above in reference to claim 9. Gillingham and Keeth did not discuss the details of the memory module regarding capacitors.

31. Moyal discloses a system comprising a capacitor having a capacitance that is selected to compensate for capacitive loading; the capacitor being coupled to a junction of a signal line and a return path [fig.4; col.2, ll.1-11].

32. It would have been obvious to one of ordinary skill in the art, having the teachings of Gillingham, Keeth and Moyal before him at the time the invention was made, to modify the memory system taught by Gillingham and Keeth to include the teachings of Moyal, in order to obtain the memory system wherein the memory module further includes a capacitor having a capacitance that is selected to compensate for capacitive loading on the data bus by the memory device of the memory module; the capacitor being coupled to a junction of the first clock signal line and the return path. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce phase mismatches [Moyal: col.2, ll.1-11].

33. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham and Keeth as applied to claim 11 above, and further in view of Wada et al., US Patent 5379248, hereinafter Wada.

34. Gillingham and Keeth taught each and every limitation as discussed above in reference to claim 11. Gillingham and Keeth did not disclose explicitly that the first and second return clock signal lines are crossed on the motherboard between the first and second modules.

35. Wada discloses a memory system wherein a first and second signal lines [bit lines] are crossed between a first and second modules [peripheral circuits] [abstract].

36. It would have been obvious to one of ordinary skill in the art, having the teachings of Gillingham, Keeth and Wada before him at the time the invention was made, to modify the memory system taught by Gillingham and Keeth to include the teachings of Wada, in order to obtain the memory system wherein the first and second return clock signal lines are crossed on the motherboard between the first and second modules. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase the freedom of circuit line layout [Wada: abstract].

37. Claim 13-15 and 22-24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham and Keeth as applied to claim 11 above, and further in view of Yoshitake, US Patent 6043704.

38. Gillingham and Keeth taught each and every limitation as discussed above in reference to claim 11. Gillingham and Keeth did not discuss the details of a dummy load regarding the memory modules [Gillingham: col.13, ll.20-37; col.15, l.60 – col.16, l.46].

39. Yoshitake discloses a system wherein a return clock signal line [clock wiring line] is coupled to a dummy load [31] [col.10, ll.56-64].

40. It would have been obvious to one of ordinary skill in the art, having the teachings of Gillingham, Keeth and Yoshitake before him at the time the invention was made, to modify the memory system taught by Gillingham and Keeth to include the teachings of Yoshitake, in order to obtain the memory system wherein the first return clock signal line is coupled to a dummy load on the second memory module and wherein the second return clock signal line is coupled to a dummy load on the first memory module. One of ordinary skill in the art would have been

motivated to make such a combination as it provides a very well known way to correct clock skews [Yoshitake: col.10, ll.56-64] and match input capacitance [Gillingham: col.13, ll.20-37].

41. As to claims 14 and 23, Yoshitake discloses, wherein the dummy load comprises a load capacitor or a dummy pin [col.10, ll.56-64; 31 contains capacitance load].

42. As to claim 15, Yoshitake discloses, wherein the dummy load is selected to match the capacitance loading of a data bus [multiple clock wiring lines constitute a bus as is well known in the art] [col.10, ll.56-64; 31 adjusted to match capacitance in order to adjust skew].

43. As to claim 22, Yoshitake discloses, comprising a control buffer [second buffers] mounted to a first side of a memory module [10 contains RAM], and further comprising a dummy load [31] for coupling to a first signal line of the control buffer to provide load matching with a load experienced by a second signal line of memory devices [third buffers] mounted to both first and second sides of the memory module [col.3, l.54 – col.5, l.63; col.10, ll.56-64].

44. As to claim 24, Keeth discloses, wherein the first signal line comprises the first clock signal or the second clock signal [e.g., dclk0], and wherein the second signal line comprises the data bus [dq] or the first clock signal [fig.4].

45. Claim 57 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham and Keeth as applied to claim 1 above, and further in view of Chan et al., US Patent 5998860, hereinafter Chan.

46. Gillingham and Keeth taught each and every limitation as discussed above in reference to claim 1. Gillingham discloses a memory module [170] coupled to the controller, the memory module having a first face including memory devices [174, 100] on the first face and including a control and address buffer on the first face, the memory module receiving the first clock signal,

the address signal and the control signal that includes a read or write command [col.2, ll.16-47; col.3, ll.1-12; fig.13, 14]. Gillingham and Keeth did not discuss a double-sided configuration for the memory module.

47. Chan discloses a memory module [20] having first and second faces including memory devices [50] on both first and second faces [fig.1, 2].

48. It would have been obvious to one of ordinary skill in the art, having the teachings of Gillingham, Keeth and Chan before him at the time the invention was made, to modify the memory system taught by Gillingham and Keeth to include the teachings of Chan, in order to obtain the memory system comprising a memory module coupled to the controller, the memory module having first and second faces including memory devices on both first and second faces and including a control and address buffer on the first face, the memory module receiving the first clock signal, the address signal and the control signal that includes a read or write command. One of ordinary skill in the art would have been motivated to make such a combination as it provides a very well known way to meet space constraints [Chan: col.1, ll.44-64; col.3, ll.4-13].

Conclusion

49. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additionally cited U.S. patent documents describe various methods and systems associated with memory modules.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
July 12, 2005